100. The conductive layer **101**, such as a metal layer, and the grounding plug **114***h* are insulated from the device substrate **100** and the array of the optoelectronic devices **102**. In particular, each grounding plug **114***b* is insulated from the device substrate **100** by a dielectric layer **112** surrounding the grounding plug **114***b*. A corresponding grounding pad **116***b* and a corresponding grounding ball **118***b* are successively disposed on the grounding plug **114***b* and opposite to the conductive layer **101**. An array of plugs **114***a* is disposed in the device substrate to electrically connect to the array of the optoelectronic devices **102**. Similar to the grounding plug **114***b*, each plug **114***a* is insulated from the device substrate **100** by a dielectric layer **112** surrounding the plug **114***a*. Moreover, an array of bonding pads **116***a* and a ball grid array (BOA) **118***a* are successively disposed on the array of plug **114***b* and opposite to the array of the optoelectronic devices **102**.

[0016] The transparent substrate **160**, such as a glass or quartz substrate, comprises a dam portion **160***a* attached to the device substrate **100**. The dam portion **160***a* of the transparent substrate **160** is attached to the device substrate **100** by an adhesion layer **110** and forms a cavity **160***b* between the device substrate **100** and the transparent substrate **160**. The micro-lens array **104** is disposed on the device substrate **100** and within the cavity **160***b*.

[0017] The lens set **126** comprising a stack of multiple lenses is mounted on the package module. The conductive layer **134**, such as a metal layer, covers the sidewalls of the lens set **126** and the package module and extends to the upper surface of the lens set **126**, having an opening **140** allowing light (not shown) to reach the array of optoelectronic devices **102**. Moreover, the conductive layer **134** is electrically connected to the grounding plug **114***b* by directly contacting the conductive layer **101** for EMI protection. In the embodiment, an opaque layer **136** comprising, for example, of opaque paint, may cover the conductive layer **134** to serve as a light shielding layer. Alternatively, a transparent conductive layer **130**, such as an indium tin oxide (ITO) or indium zinc oxide (IZO) conductive layer, may optionally be disposed on the upper surface of the lens set **126** and be covered by the conductive layer **134** to further enhance EMI protection; while also being capable of allowing light to reach the array of optoelectronic devices.

[0018] FIGS. **1**A to **1**H are cross sections of an exemplary embodiment of a method for fabricating an electronic assembly for an image sensor device according to wafer level CSP technology. As shown in FIG. **1**A, a device wafer/substrate **100** comprising silicon or other semiconductor material is provided. The device wafer **100** comprises a plurality of arrays of optoelectronic devices **102**, such as pixel diodes, formed therein. Each array of optoelectronic devices **102** is isolated from each other by a plurality of conductive layers **101**, such as metal layers. Each conductive layer **101** is insulated from the device wafer **100** by a dielectric layer (not shown) and is not electrically connected to any array of optoelectronic devices **102**. A transparent wafer/substrate **160**, such as a glass or quartz substrate, comprising a plurality of dam portions **160***a* is attached to the device wafer **100** by an adhesion layer **110**, thereby forming cavities **160***b* between the device wafer **100** and the transparent wafer **160**. Prior to bonding the transparent wafer **160** on the device wafer **100**, a plurality of micro-lens arrays **104** is formed on the device substrate **100** corresponding to cavity **160***b*, such that each micro-lens array **104** can be disposed within the corresponding cavity **160***b* after bonding the transparent wafer **160** on the device wafer **100**.

[0019] Referring to FIG. **1**B, the device wafer **100** is thinned down by polishing. Next, the device wafer **100** is etched to form via holes **103***a*, **103***b*, and **103***c*. The via hole **103***a*, arranged in a plurality of arrays, exposes the corresponding arrays of optoelectronic devices **102**. The via holes **103***b* and **103***c* exposes the conductive layers **101**. In particular, the via hole **103***c* serves as scribe lines of the device wafer **100**.

[0020] Referring to FIG. **1**C, a dielectric layer **112** is formed on the inner sidewall of each of the via holes **103***a*, **103***b*, and **103***c*. The via holes **103***a* and **103***b* are subsequently filled with a conductive material, such as metal, to form arrays of conductive plugs **114***a* electrically connected to the arrays of optoelectronic devices **102** and grounding plugs **114***b* electrically connected to the conductive layers **101**. The arrays of conductive plugs **114***a* and grounding plugs **114***b* are insulated from the device wafer **100** by the dielectric layer **112**. After formation of the arrays of conductive plugs **114***a* and grounding plugs **114***b*, the arrays of bonding pads **116***a* are formed on the corresponding arrays of conductive plugs **114***a* and the grounding pads **116***b* are formed on the corresponding grounding plugs **114***b*. Next, a protective layer **120**, such as a solder mask, is formed on the lower surface of the device wafer **100** and on the sidewall of the via holes **103***c*, exposing the arrays of bonding pads **116***a* and the grounding pads **116***b*.

[0021] Referring to FIG. **1**D, solder ball placement process is performed to form grounding balls **118***b* on the corresponding grounding pads **114***b* and ball grid arrays **118***a* are formed on the corresponding arrays of bonding pads **116***a*.

[0022] Referring to FIG. **1**E, a lens set **126** is subsequently mounted on the transparent wafer **160**. In this embodiment, the lens set **126** comprises a stack of multiple lenses and does not use a housing or holder for mounting the lens set onto the transparent wafer **160**. A transparent conductive layer **130**, such as an ITO or IZO layer, is optionally deposited on the upper surface of the lens set **126**. Next, a masking pattern layer **132**, such as a photoresist or resin layer is formed on the transparent conductive layer **130** corresponding to each micro-lens array **104**.

[0023] Referring to FIG. **1**F, a dicing process is performed along the via holes **103***c* serving as scribe lines of the device wafer **100** to form a plurality of CSP modules with a lens set **126** thereon. A portion of the conductive layer **101** in the device substrate **100** is thus exposed after the dicing process.

[0024] Referring to FIG. **1**G, a conductive layer **134**, such as a metal layer, is formed on the sidewall and upper surface of each CSP module with a lens set **126**, as shown in FIG. **1**F, to cover the transparent conductive layer **130** and the masking pattern layer **132**. In order to simplify the diagram, only one CSP module with a lens set **126** is depicted. The conductive layer **134** on the sidewall of the device substrate **100** is in direct contact with the exposed conductive layer **101**, thereby electrically connecting the grounding balls **118***b* through the grounding plugs **114***b* and the grounding pads **116***b*. An opaque layer **136** comprising, for example, of opaque paint, is formed on the conductive layer **134** to serve as a light shielding layer.

[0025] Referring to FIG. **1**H, the masking pattern layer **132** and the opaque and conductive layers **136** and **134** thereon are removed from the transparent conductive layer **130**, thereby